CL-307 Product Family Specification

PFS-CL307-A1

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INTELLIGENT VEHICLE CONTROLS HED

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USING THIS DOCUMENT

The specifications contained herein represent all possible configurations for this product family. The actual configurations available on each module may be a subset of this specification. Please refer to the module-specific datasheet for the connector pinout and configurations that are available.

USER LIABILITY

The OEM of a machine or vehicle in which HED® electronic controls are installed is fully responsible for all consequences that might occur. HED®, and any authorized distributor, has no responsibility for any consequences, direct or indirect, caused by failures or malfunctions. Failure or improper selection or improper use of HED® products can cause death, personal injury and property damage.

The OEM must analyze all aspects of their application and review the information concerning product or system in the current product documentation. Due to the variety of operating conditions and applications for these products or systems, the user, through its own analysis and testing, is solely responsible for making the final selection of the products and systems and assuring that all performance, safety and warning requirements of the application are met.

The products described herein, including without limitation, product features, specifications, designs, availability and pricing, are subject to change by HED® at any time without notice.

INPUT VTD (PINS B08–B10)

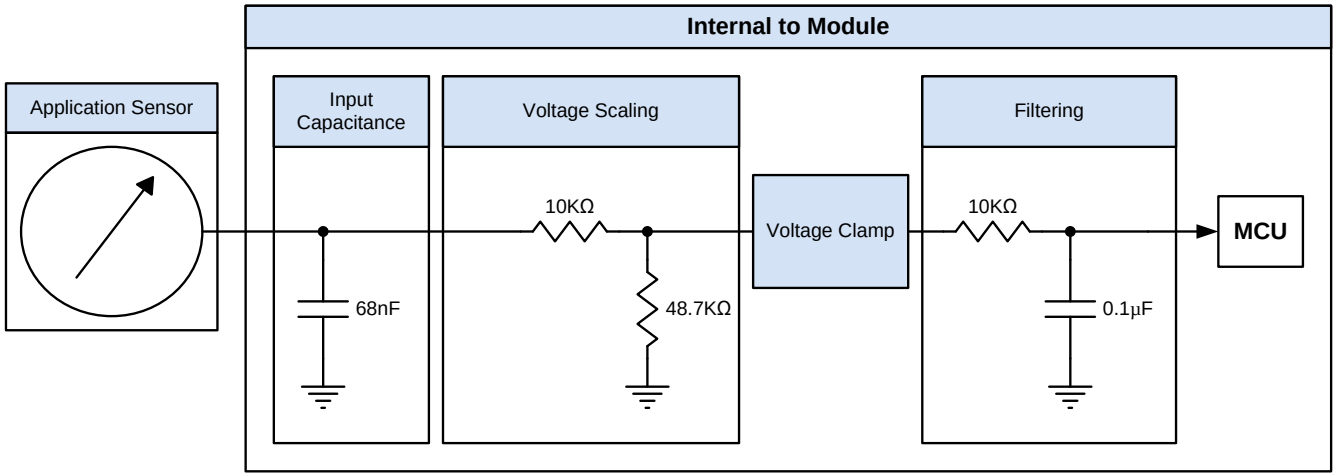
Voltage-to-Digital (VTD)
(0 – 5.61VDC)

Input Voltage Range
- 0V to 5.47V (minimum)
- 0V to 5.61V (typical)

Input Resistance
- 58.7KΩ (typical)

Resolution
- 12 Bits
- 1.37mV / count (typical)

Accuracy[1]
- ±1.0% and ±6mV (T_A = 25°C)
- ±2.0% and ±71mV (T_A = Full)



[1] VTD accuracy is estimated using datasheet maximums and a weighted average of worst-case and root-sum-square (RSS) methods. It is considered as a percentage of the input voltage combined with an additional offset.

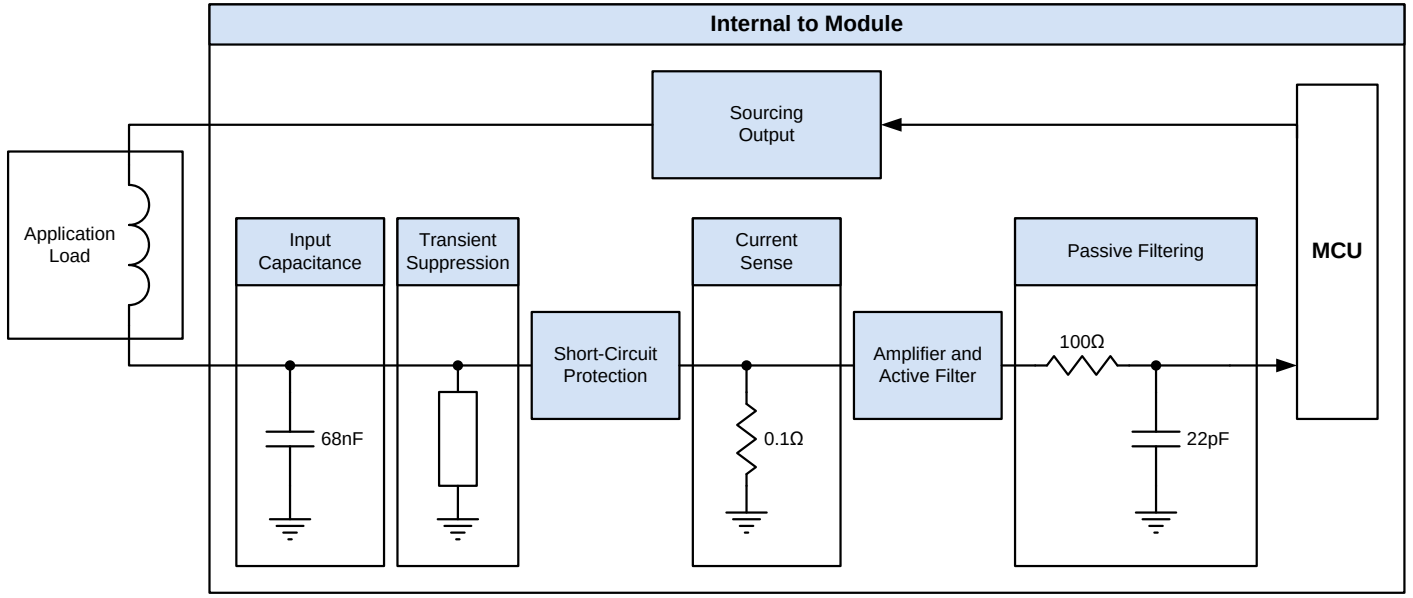
RETURN(-) OUTPUTS (PINS A11, A12, B01, B02)

Current Sense Range
- 0A to 3.43A (minimum)
- 0A to 3.69A (typical)

Resolution
- 12 Bits
- 0.90mA / count (typical)

Hardware Current Limit / Trip Point
- 3.9A (minimum)
- 5.2A (typical)
- 5.8A (maximum)

Accuracy[1]
- ±1.0% and ±10mA (T_A = 25°C)
- ±3.0% and ±25mA (T_A = Full)



[1] Return(-) Output accuracy is estimated using datasheet maximums and a weighted average of worst-case and root-sum-square (RSS) methods. It is considered as a percentage of the return current combined with an additional offset. These values assume factory calibration.

INPUT STG/FREQ (PINS B11–B12)

Switch-to-Ground (STG) Mode

Pull-up Resistance
- 389Ω (typical)

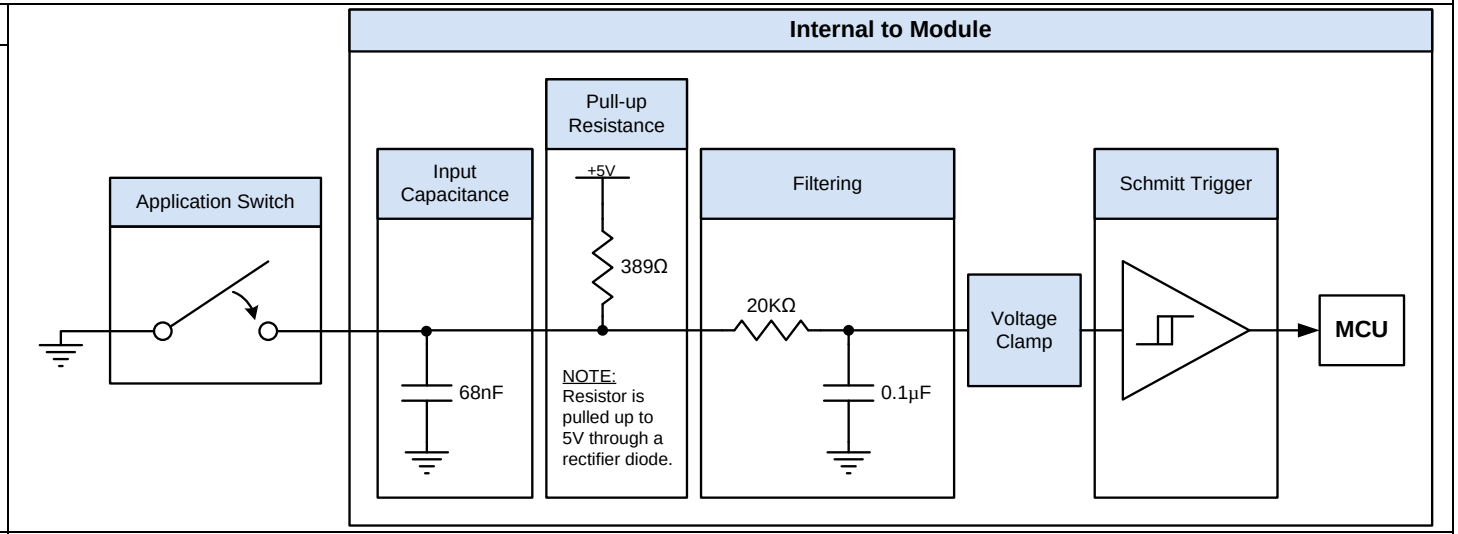
Input Current
- 10.9mA at 0V (typical)

Positive Going Threshold
- > 3.5V

Negative Going Threshold
- < 1.5V

Parallel Resistance
- 2KΩ at 0V (minimum)

Series Resistance
- 220Ω (maximum)



Frequency / PWM / Encoder Mode

Pull-up Resistance
- 3.92KΩ (typical)

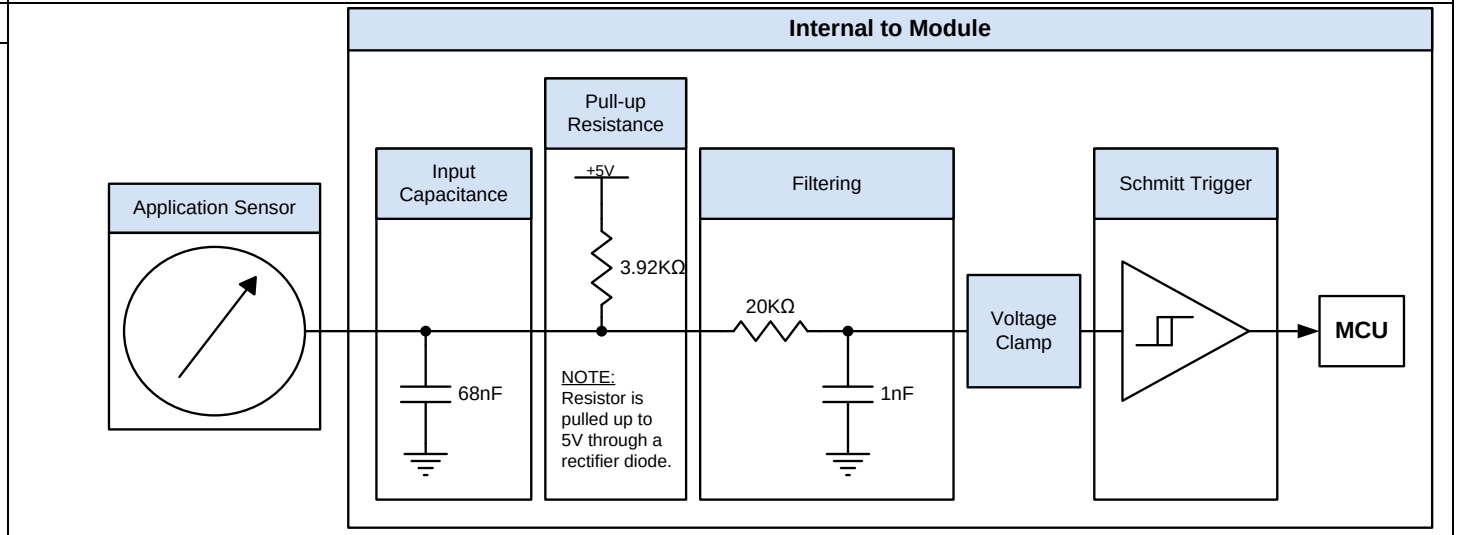
Positive Going Threshold
- > 3.5V

Negative Going Threshold
- < 1.5V

Frequency Range
- 1KHz (maximum)[1]
- 10KHz (maximum)[2]

Resolution
- < 5 Hz

Accuracy
- ±2.0% (T_A = full range)



[1] Frequency range maximum assumes square wave, open-drain, sinking sensor at 50% duty cycle.
[2] Frequency range maximum assumes square wave, active push-pull sensor at 50% duty cycle.

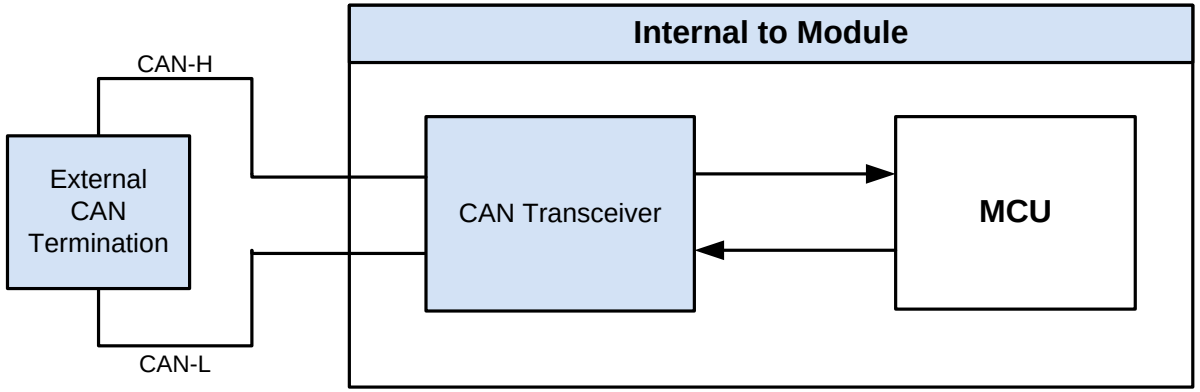
CAN COMMUNICATION (PINS A03/A04)

Baud Rate
- 40kbps to 250kbps

Maximum Allowable Voltage[1]
- -80V to +80V

Input Capacitance (maximum)
- 20pF (f = 1MHz)

No Internal Termination



[1] Maximum allowable voltage defines the voltage extremes that the transceiver can tolerate. Exposure to these voltages for extended periods may affect device reliability.

OUTPUT DOUT(+)/PWM(+)/ECC(+) (PINS A07-A10, B03-B06)

Individual Output Current[1]
- Digital Mode = 3.0A (maximum)
- PWM Mode = 3.0A (maximum)

Grouped Output Current[2,3,4]
- Digital Mode = 2.5A (maximum)
- PWM Mode = 2.0A (maximum)

PWM Frequency[5]
- < 300 Hz (typical)
- < 1 KHz (maximum)

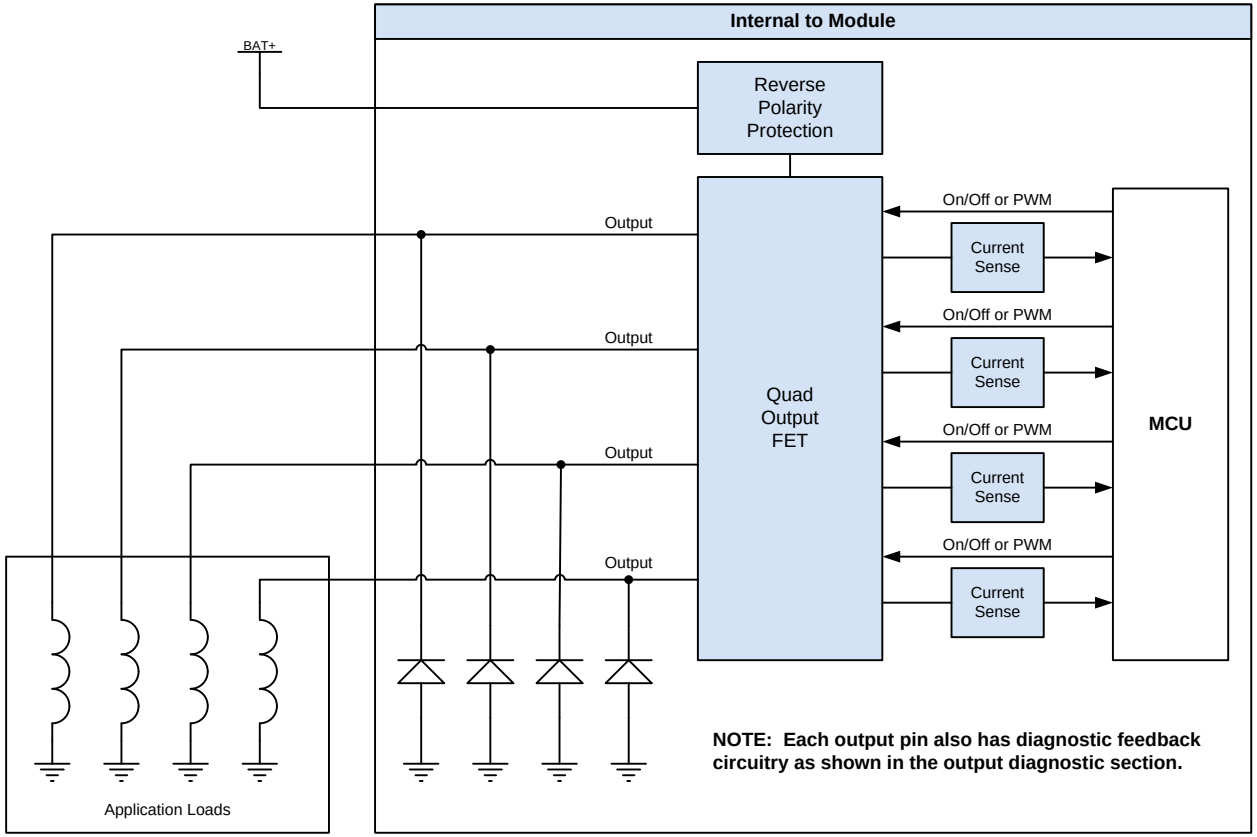
Output Diagnostics
- Short to Battery
- Short to Ground
- Overcurrent
- Open Circuit[6]

Current Sense Range
- Up to 3.5A (minimum)
- Up to 4.4A (typical)

Current Sense Resolution
- 12 bits
- 1.1mA / count (typical)

Current Sense Accuracy (typical)
- ±50mA at 2A, T_A = 25°C

Internal Flyback Diodes



[1] Individual Output Current specifies the maximum current for an individual output channel. Additional restrictions regarding total output current, number of active channels, etc. will apply and are specified in the Grouped Output Current parameter. PWM outputs assume 250Hz frequency.

[2] Output current is constrained in groups of four pins (quad output FET). Pin groups are A07-A10 and B03-B06. It is strongly recommended to level the total output current across each of the groups for best thermal performance.

[3] Output current maximums assume all four channels are active simultaneously and the module is at maximum ambient temperature. PWM outputs assume 250Hz frequency. Output current may be increased per channel (up to the individual output current maximum) if not all channels are active simultaneously or other channels are at a reduced load current. Please contact HED® for further information.

[4] Maximum total output current for Pins A07-A10 is 10 Amps. Maximum total output current for Pins B03-B06 is 10 Amps.

[5] The output driver is best suited for PWM frequencies of 300 Hz or less. PWM frequencies of up to 1 KHz are possible, but at reduced output current and duty cycle range.

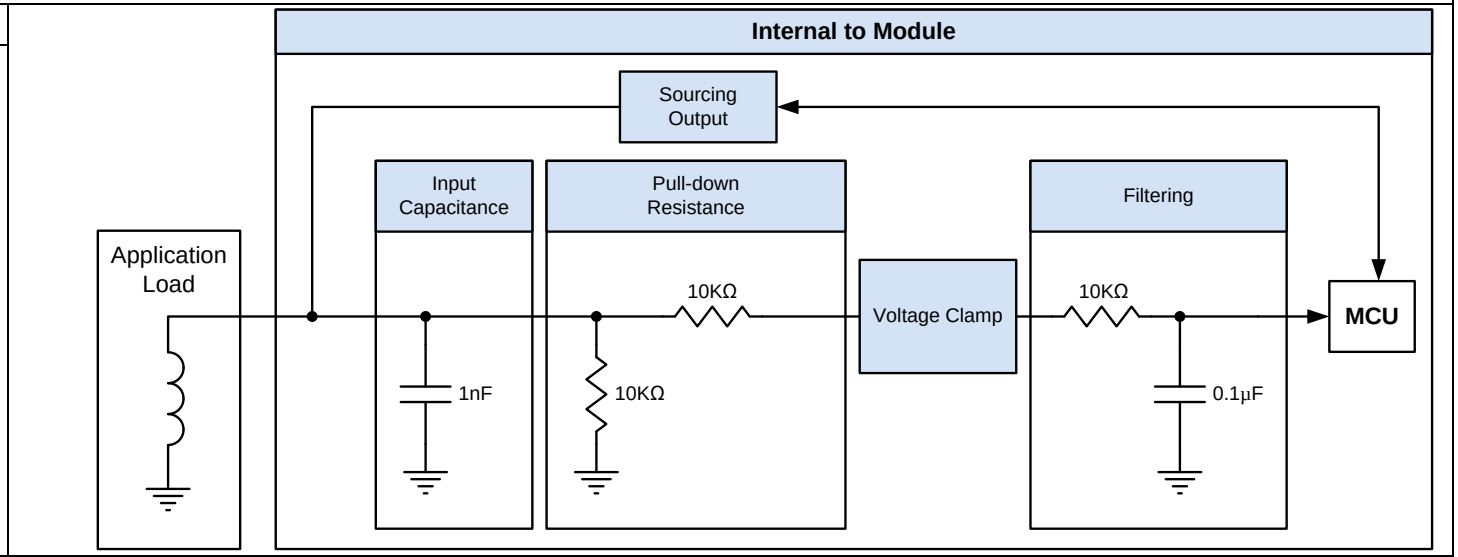
[6] Open circuit can be detected when the output is active using current sense feedback for load currents of at least 250mA and duty cycle of 100%. Open circuit can be detected when the output is inactive using the pull-up resistor for loads that are not influenced by the associated pull-up current (see Open Circuit Detection Mode circuit diagram).

OUTPUT DIAGNOSTICS (PINS A07-A10, B03-B06)

Normal Mode

Pull-down Resistance
- 10KΩ (typical)

Pull-down Current
- 1.1mA at 8V (typical)
- 5.9mA at 32V (typical)

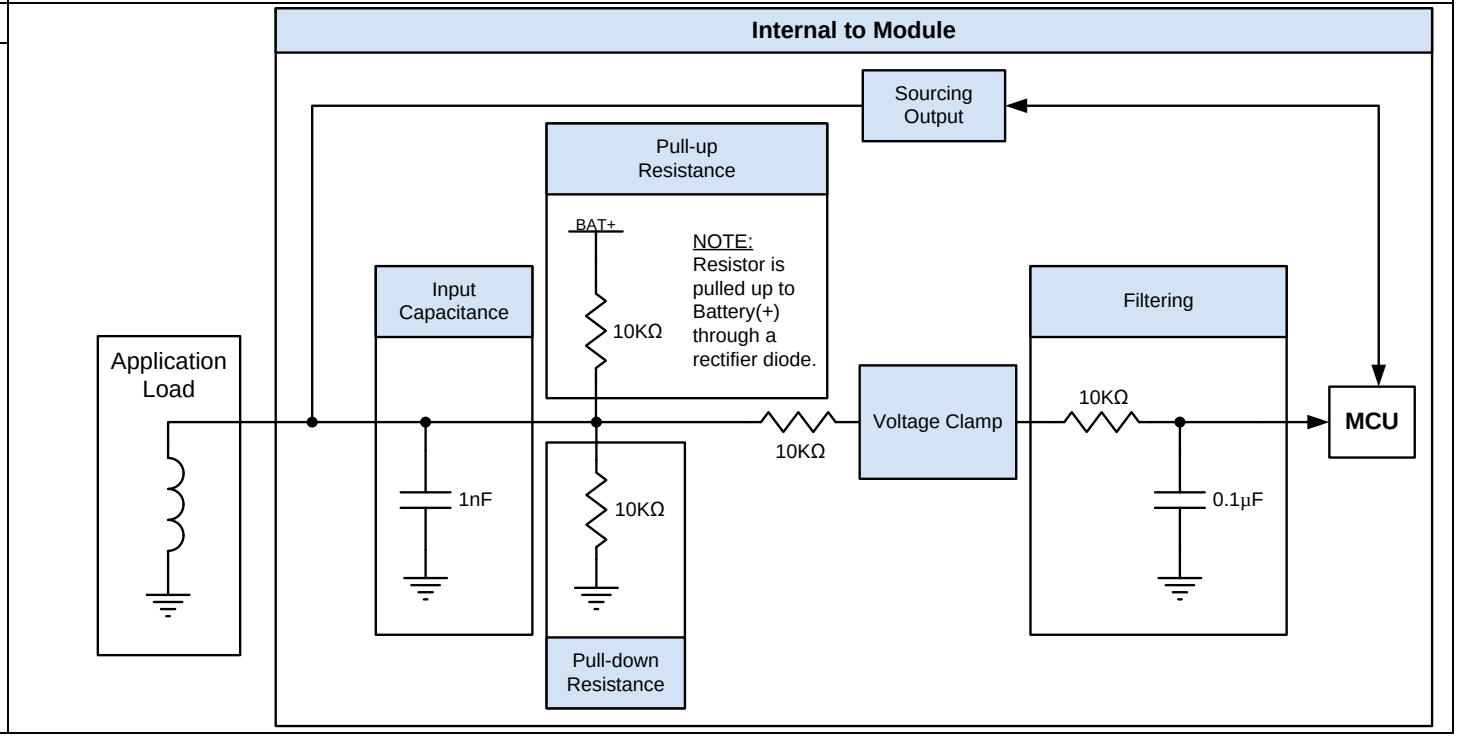


Open Circuit Detection Mode

Pull-down Resistance
- 10KΩ (typical)

Pull-up Resistance
- 10KΩ (typical)

Pull-up Current (assume < 100Ω load)
- 0.7mA at 8V (typical)
- 3.1mA at 32V (typical)



BATTERY (+) MODULE (PIN A06) AND BATTERY (+) OUTPUTS (PINS A05, B07)[1]

Battery (+)

Operating Voltage Range
- 8VDC – 32VDC

Maximum Continuous Voltage[2]
- 36VDC

Module Current Draw[3]
- 71mA at 8.0V (typ)
- 43mA at 13.8V (typ)
- 27mA at 28.0V (typ)
- 25mA at 32.0V (typ)

Maximum Total Output Current
- See Output Section for output current constraints

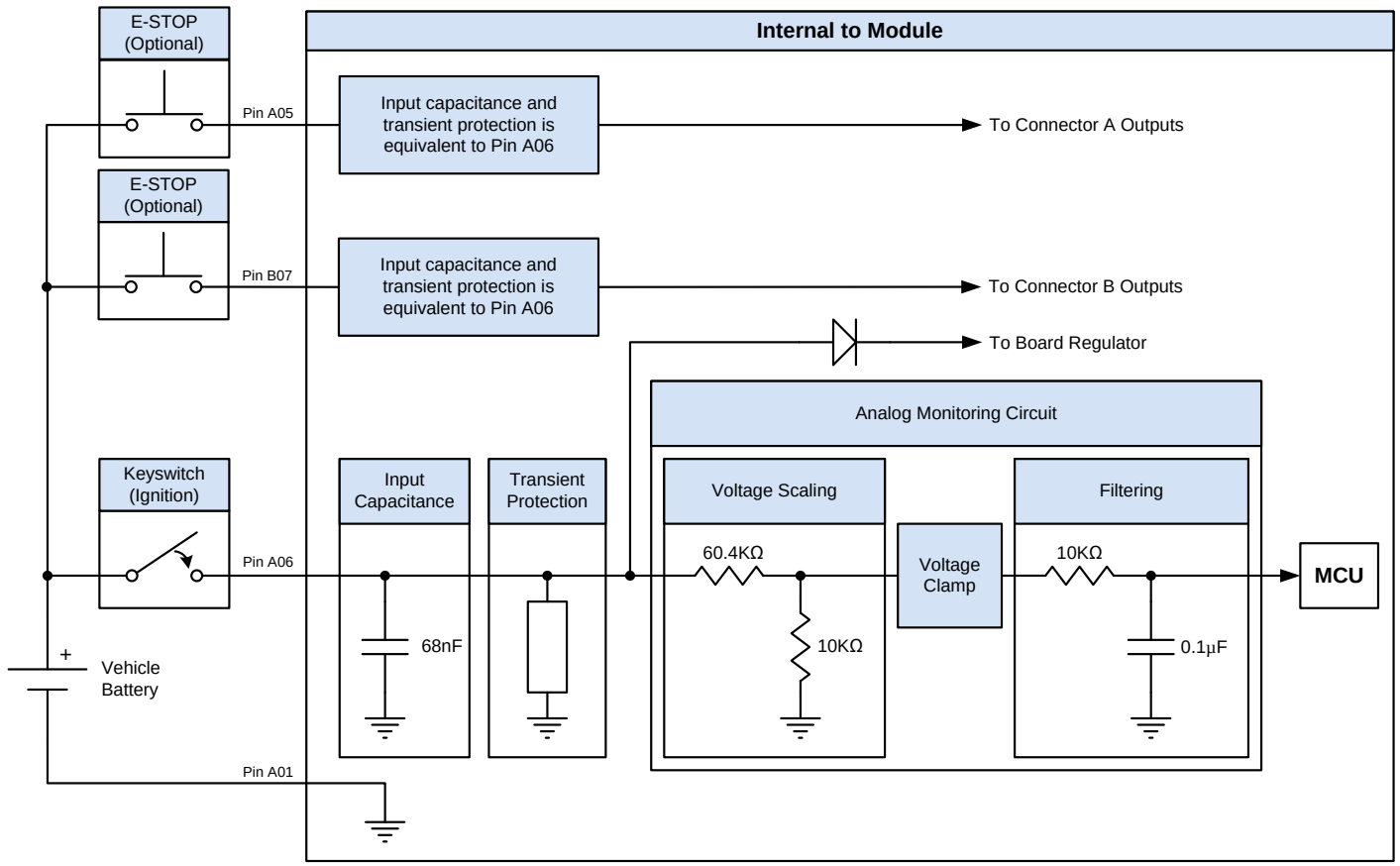
Analog Monitoring Circuit

Input Voltage Range
- 0V to 32.46V (minimum)
- 0V to 32.79V (typical)

Input Resistance
- 70.4KΩ (typical)

Resolution
- 12 Bits
- 8.00mV / count (typical)

Accuracy[4]
- ±1.5% and ±35mV (T_A = 25°C)
- ±3.5% and ±405mV (T_A = Full)



[1] The block diagram shown represents one possible implementation in the system. Other implementations may be used based on system requirements.
[2] Exposure to maximum voltages for extended periods may affect device reliability.
[3] Module current draw is measured with I/O inactive and no CAN communication.
[4] VTD accuracy is estimated using datasheet maximums and a weighted average of worst-case and root-sum-square (RSS) methods. It is considered as a percentage of the input voltage combined with an additional offset.

ADDITIONAL NOTES

IMPORTANT: Module configurations that contain sourcing outputs with internal flyback diodes may continue to operate in the event of a loss of module ground. This event can result in a ground shift to the internal board reference (ground). The ground shift is a result of a remaining current path from internal board reference (ground), through internal flyback diode(s), and terminating through an external load to ground (assuming the load is of relatively low resistance). Depending on system configuration and load resistances, analog input accuracy can be affected, especially if the analog sensor is not referenced to the module sensor ground. Be sure to include this condition when conducting a system-level FMEA.

REVISION HISTORY

Revision	Date	EC #	Changes
A1	06/19/15	315-003	Initial Release.